PERANCANGAN SISTEM DIGITAL

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TEKNIK ELEKTRO
UNIVERSITAS ISLAM “45”
BEKASI
**Topic 9**

**JTAG Boundary-Scan**

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(Based on Ben Bennetts’ Tutorial)

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**Sources & Background**

- JTAG Boundary Scan is from IEEE Standard 1149.1
- Most of slides here are based on the document “Boundary Scan Tutorial” by Ben Bennetts, for ASSET InterTech Inc.,  
ww.asset-intertech.com/pdfs/boundaryscan_tutorial.pdf

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**Problem with modern packaging styles**

- In-Circuit & Functional Board Test
- Bed-Of-Nails (MDA, ICT)  
Functional

- DIP  
PGA  
SOIC  
TSOP  
SOJ  
PLCC  
QFP  
BGA
Problem with multi-layer PCB

Motivation of Boundary Scan
- Basic motivation was miniaturization of device packaging, leading to ...
- surface mount packaging styles, leading to ...
- double sided boards, leading to ...
- multi-layer boards, leading to ...
- a reduction of physical access test lands for traditional bed-of-nail in-circuit testers

- Problem: how to test for manufacturing defects in the future?
- Solution: add boundary-scan registers to the devices

Principle of Boundary Scan

The Boundary Scan Path
**Basic Boundary Scan Cell**

- Data In (PI)
- Capture Scan Cell
- Update Hold Cell
- Scan In (SI)
- Clock DR (Clk DR)
- Update DR
- Data Out (PO)
- Mode = 0, Functional mode (for BC_1)
- Mode = 1, Test mode

**Defect Coverage: Bed-of-nails**


**Defect Coverage: Extest**

In this mode (EXternal TEST), defects covered:
- driver (TX) scan cell - driver amp - bond wire - leg - solder - interconnect - solder - leg - bond wire - driver amp - sensor (RX) scan cell

**Defect Coverage: Intest**

In this mode (INternal TEST), defects covered:
- driver scan cell - device - sensor scan cell
1149.1 Chip Architecture

Mandatory Instructions and Reset Modes

Target Register Modes

Open-Circuit TDI, TMS and TRST*?

- An open-circuit TDI, TMS or TRST* must go to logic-1. Why?
- TDI: Bypass instruction is loaded: safe instruction
- TMS: TAP controller placed into Test Logic Reset state after 5 TCKs, max: safe state
- TRST* not asserted. Rest of 1149.1 logic still usable
**Instruction Register**

- DR select and control signals routed to selected target register

**Standard Instructions**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Selected Data Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mandatory:</td>
<td></td>
</tr>
<tr>
<td><strong>Exttest</strong></td>
<td>Boundary scan (formerly all-0s code)</td>
</tr>
<tr>
<td><strong>Bypass</strong></td>
<td>Bypass (initialised state, all-1s code)</td>
</tr>
<tr>
<td><strong>Sample</strong></td>
<td>Boundary scan (device in functional mode)</td>
</tr>
<tr>
<td><strong>Preload</strong></td>
<td>Boundary scan (device in functional mode)</td>
</tr>
<tr>
<td>Optional:</td>
<td></td>
</tr>
<tr>
<td><strong>Intest</strong></td>
<td>Boundary scan</td>
</tr>
<tr>
<td><strong>Idcode</strong></td>
<td>Identification (initialised state if present)</td>
</tr>
<tr>
<td><strong>Usercode</strong></td>
<td>Identification (for PLDs)</td>
</tr>
<tr>
<td><strong>Runbist</strong></td>
<td>Result register</td>
</tr>
<tr>
<td><strong>Clamp</strong></td>
<td>Bypass (output pins in safe state)</td>
</tr>
<tr>
<td><strong>HighZ</strong></td>
<td>Bypass (output pins in high-Z state)</td>
</tr>
</tbody>
</table>

NB. All unused instruction codes must default to **Bypass**

**Extest Instructions**

- Boundary-scan register selected
- Used to apply patterns to the interconnect structures on the board
- Boundary-scan cells have permission to write to their outputs (device in test mode)

**Bypass Instruction**

- Bypass register selected
- Used to allow quick passage through this device to another device connected in the chain
Sample and Preload Instruction

- Boundary scan register selected
- Used to Preload known values in the boundary scan cells.
- Also used to Sample (Capture) mission-mode signals into the boundary-scan cells
- Device in functional mode, not test mode

Intest Instruction

- Boundary scan register selected
- Used to apply patterns to the device itself
- Boundary scan cells have permission to write to their outputs (device in test mode)

Idcode Instruction

- Optional Identification register selected, if available, else Bypass register selected
- Used to capture internal 32-bit identification code (manufacturer, part number, version number) and then shift out through TDO

Usercode Instruction

- Optional Identification register selected, if available, else Bypass register selected
- Use to capture an alternative 32-bit identification code for dual personality devices e.g. PLDs
RunBIST Instruction

- Control registers for initiating internal BIST (Memory or Logic)
- Pass/fail register targeted as final selected register

Clamp Instruction

- Known values are pre-loaded into boundary scan cells using **Preload** instruction
- **Clamp** drives these values to the output pins but leaves Bypass register as the selected register

HighZ Instruction

- Control-to-Z values are pre-loaded into high-Z control cells using the **Preload** instruction
- **HighZ** drives these values to the three-state controls causing them to go to their high-Z drive state but leaves Bypass register as the selected register

Test Access Port (TAP)

- **Test Data In** (TDI) Serial data in, Sampled on rising edge, Default = 1
- **Test Data Out** (TDO) Serial data out, Sampled on falling edge, Default = Z (only active during a shift operation)
- **Test Mode Select Input Control** (TMS) Sampled on rising edge, Default = 1
- **Test Clock** (TCK) Dedicated clock, Any frequency
- **Test Reset** (TRST*) Optional async reset, Active low, Default = 1
**TAP Controller**

- TMS
- TCK
- TRST*

- 16-state FSM
- TAP Controller
- (Moore machine)

- ClockDR
- ShiftDR
- UpdateDR
- Reset*
- Select
- ClockIR
- ShiftIR
- UpdateIR
- Enable

**TAP Controller State Diagram**

**Bypass Register**

- One-bit shift register, selected by the *Bypass* instruction
- Captures a hard-wired 0
- Note: in the Test-Logic/Reset state, the Bypass register is the default register if no Identification Register is present

**Identification Register**

- 32-bit shift register
- Selected by *Idcode* and *Usercode* instruction
- No parallel output
- Captures a hard-wired 32-bit word
- Main function: identify device owner and part number
- Note: *Idcode* is power-up instruction if Identification Register is present, else *Bypass*
Boundary Scan Register

- Shift register with boundary-scan cells on:
  - device input pins
  - device output pins
  - control of three-state outputs
  - control of bidirectional cells
- Selected by the \textit{Extest, Intest, Preload} and \textit{Sample} instructions

Boundary Scan Cell OZ

On all device signal IO, control of three-state: \textit{dual-mode input signal} or additional scan cell

Boundary Scan Cell IO

On control of bidirectional IO: \textit{dual-mode input signal}

Application at Board Level

1. BS infrastructure integrity test
2. Interconnect test
3. Non-BS device test, including RAM test
Board Defects

- Missing component, wrong component, mis-oriented component, broken track, shorted tracks, pin-to-solder open circuit, pin-to-pin solder shorts
- Number of 2-net short circuit faults between k interconnects = \( k(k-1)/2 \)
- Equivalent fault models for shorts: bridging of type wired-AND and wired-OR
- Open circuits are modelled downstream as stuck-at-1 or stuck-at-0 faults

Example of faults

Generating Open and Short Test

Chip 1

Wired-OR Short

Chip 2

Net 1

Net 2

Net 3

Net 4

s-a-0 Open

Parallel update

s-a-0 Open

Parallel capture

Scan-in stimulus 1011

Generate test response 0111

How many tests are needed?

- Determine a set of tests to detect all:
  - open circuits, modelled as any net s-a-1 and s-a-0, and
  - short circuits, modelled as all 2-net shorts of type wired-AND and wired-OR i.e. \{1,2\}, \{1,3\}, \{1,4\}, \{2,3\}, \{2,4\}, \{3,4\}
Building the tests

- Each code has at least one 1, one 0
- 2 forbidden codes: all-1's, all-0's
- 2-net shorts: each code is unique

Determine a set of tests to detect all:
- open circuits, modelled as any net s-a-1 and s-a-0, and
- short circuits, modelled as all 2-net shorts of type wired-AND and wired-OR
  i.e. \{1,2\}, \{1,3\}, \{1,4\}, \{2,3\}, \{2,4\}, \{3,4\}

Number of Tests

- Number of tests = \(\lceil \log_2(k + 2) \rceil\), \(k = \) number of interconnects
- 13 for \(k = 8000\) interconnects

Testing non-Boundary Scan cluster

- On modern boards, most non-boundary-scan devices are simple pass-thru devices e.g. line drivers
- Consequently, tests for presence, orientation and bonding are easily generated and easily applied via the embracing boundary-scan devices

Combining BS and Nails

- Use ICT nails to access uncontrollable/unobservable cluster-internal nets
- Select the real-nail locations on non-BS nets according to access to:
  - strategic Enables for guarding or preventing bus conflicts,
  - buried nets in non-embraced clusters,
  - other key control signals e.g. O_Enable, Bidir or 3-state control signals
RAM Array Testing via Boundary Scan

Hardware Requirement

Tool Flow for Boundary Scan Tests

Where are we today?
Spread of Design-for-Test (DFT)

<table>
<thead>
<tr>
<th>Chip</th>
<th>Board</th>
<th>System/Field Service</th>
</tr>
</thead>
<tbody>
<tr>
<td>5001-00 Emulation (eJTAG)</td>
<td>1149.1-90/93/94/01 Interconnect Test</td>
<td>Texas Inst. Nat Semi Back-Plane Bus</td>
</tr>
<tr>
<td>1500-02(?) Embedded Core Test</td>
<td>1149.4-99 Mixed-Signal Bus</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1532-00 In-System Configuration</td>
<td></td>
</tr>
</tbody>
</table>
References


